REMARKS/ARGUMENTS

35 USC §103(a) - Claim 1

Independent claim 1 is rejected in the current Office Action under §103(a) over the combination of Shu (US 5,594,839) in view of Schmidt (US 5,193,012) and Hashimoto (US 4,999,814). Of note in this rejection is that Hashimoto is contended as teaching the feature of *"steps (a) to (c) are performed simultaneously with step (d)"*.

Applicant has reviewed the detailed explanation provided by the Examiner in the *"Response to Arguments"* section of the instant Office Action, and thanks the Examiner for this detailed explanation. However, Applicant respectfully disagrees that the above combination of Shu, Schmidt, and Hashimoto teach the claimed invention, particularly with regards to the feature of *"steps (a) to (c) are performed simultaneously with step (d)"*.

Applicant very respectfully submits that the Examiner's interpretation and understanding of Hashimoto is incorrect.

A brief summary of steps (a) to (c) and (d) of claim 1 is firstly provided. Step (a) of claim 1 recites that a plurality of dither values are read from a memory. Step (c) recites that these values are then output into a buffer memory . Step (d) recites that dither values in the buffer memory are then output. The last paragraph of claim 1 recites that steps (a) - (c) are performed simultaneously with step (d). In other words, dither values are output into the buffer memory simultaneously with dither values being output from the buffer memory.

In the rejection, the Examiner maintains that Hashimoto discloses a simultaneous output into and output from a buffer memory. The Examiner refers, for example, to the descriptions of Hashimoto at col. 1, lines 61 - 66, col. 2, lines 10 - 51, and col. 6, lines 31 - 40. Applicant's following remarks explain why these portions of Hashimoto do not in fact teach simultaneous reading and writing to/from a buffer.

Col. 1, lines 61 - 66

This portion of Hashimoto describes that sense amplifiers are provided with the write line buffer and read line buffer for parallel input and output, respectively. In this context, that parallel input and parallel output do not mean that input and output are performed simultaneously.

Rather, "parallel input" means that data is inputted in parallel as opposed to serially. Similarly, "parallel output" means that data is outputted in parallel as opposed to serially. Indeed, this is illustrated in Fig. 1, where each row and column line of the DRAM has its own connection to the write line buffer and the read line buffer.

That Examiner has mistakenly understood the description of *"...parallel input and output, respectively."* to mean that input and output are performed simultaneously.

In fact, this portion of Hashimoto does not teach or suggest simultaneous input and output of data from a buffer. The use of the word *"respectively"* in this description of Hashimoto supports Applicant's position that Applicant's interpretation of Hashimoto is the correct technical interpretation.

Col. 2, lines 10 - 51

This portion of Hashimoto describes only a write process. This description of Hashimoto does not teach or suggest simultaneous input and output of data from a buffer.

Col. 6, lines 31 - 40

Applicant firstly notes that this portion of Hashimoto is part of claim 5. Accordingly, Applicant respectfully submits that this description alone is not enabling, and accordingly does not teach or suggest the feature at issue. The claims of a patent should be supported by their description, and accordingly, the description that supports this feature of claim 5 of Hashimoto should be referred to instead of claim 5 itself.

As previously submitted, the description of Hashimoto at col. 6, lines 31 - 40, when read in its proper context in consideration of the description in the specification, suggests only that read, and write requests can be generated without interrupting a refresh procedure. This description of Hashimoto does not teach or suggest simultaneous outputting into and from a buffer memory.

The feature of claim 5 of Hashimoto is explained in more detail at col. 3, lines 23 - 48. In particular, Applicant directs the Examiner's attention to the description at col. 3, lines 26 - 31, which reads:

"For example, if write, refresh and read requests to write, refresh and read, respectively, data in the dynamic memory are generated simultaneously for execution ***in this order****, necessary data will always have been written in the read line buffer 900 nsec later."* (emphasis added)

This description very clearly illustrates that while write, refresh and read signals can be generated simultaneously, it does not mean that they are performed simultaneously. The above description explicitly states *"...for execution* ***in this order****..."*, which clearly means that such processes are not performed simultaneously.

Should the Examiner disagree, Applicant would very much appreciate the Examiner's further explanation of how the above description of Hashimoto describing *"...executing* ***in this order****..."* can suggest that the write, refresh, and read operations are in fact performed simultaneously.

Therefore, Applicant maintains that Hashimoto is completely silent as to a simultaneous output into and output from a buffer. All portions of Hashimoto relied upon by the Examiner have been shown above to not in fact teach or suggest a simultaneous output into and output from a buffer.

Still further, Applicant points out that claim 1 recites outputting dither values into a buffer memory simultaneously with outputting dither values from the (**same**) buffer memory. In contrast, Hashimoto involves two separate buffers. Namely, a write line buffer and a read line buffer.

Even if, for the sake or argument, one were to assume that Hashimoto did teach simultaneously reading writing into/from the write line and read line buffers, such an operation concerns two separate buffers and does not relate to one buffer memory. Claim 1 concerns outputting dither values into and from the same buffer memory. Accordingly, a

teaching concerning outputting data from a first buffer simultaneously with inputting data to a second different buffer does not prejudice this feature of claim 1.

Applicant acknowledges that a "buffer memory" may be made up of separate physical memory devices. However, in order for a group of separate physical memory devices to be considered as a single "buffer memory", the group should at least be able to be logically operated as a single buffer memory, and each memory device of the group should have for example the same input and output respectively.

Even if one were to group the write line buffer and read line buffer together, one could not consider this group as a single buffer memory. The read line buffer receives inputs from the DRAM and outputs to an external target, whereas the write line buffer receives input from an external source and outputs to the DRAM. They are clearly two separate buffers, and operate as such.

In view of the above, Applicant respectfully maintains that the combination of Shu, Schimdt and Hashimoto still fails to arrive at the claimed invention. In view of the above deficiencies of Hashimoto, this combination still fails to teach or suggest outputting dither values into a memory buffer simultaneous with outputting dither values from the **same** memory buffer.

Very respectfully,

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